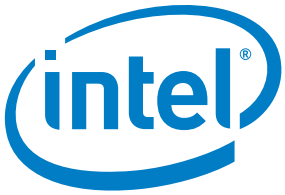

Digital Signage

Open Pluggable Specification (OPS)

Electrical, Mechanical, and Thermal Specification

June 2019

Document Number: 613108-007US

Contents

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Revision History

Document Number	Revision Number	Description	Revision Date
613108	007	Previous document number 324427 has expired. The new document number is 613108. Updated Section 4.2 by removing the Dummy Module for Thermal Test.	June 2019
324427	006	Updated JAE TX25A/24A connector information Refreshed image on Figures 1 and 3 Include Note on hot plug function requirement Added section 2.2 for JAE connector compatibility Included Note on USB3.0 implementation	June 2016
324427	005	Added Section 3.5, Dimensions of the Pluggable Module Slot on the Display Panel Added Section 3.6, Venting Area on the Display Panel for the Pluggable Module Added Section 4.2, Thermal Consideration for Display Panel	September 2012
324427	004	Added title to Notice section	June 2012
324427	003	Refreshed image on Figure 1 Added additional reference documents Updated Table 2 power rating requirement for OPS: 1. Removed recommended current rating of 500mA for each pin and updated DC IN current (A) spec to 8A max(1A per pin) 2. In-rush current of pluggable module shall not exceed 10A 3. Highlighted the requirement for manufacturers to provide power rating label on their respective (module and display panel) products Included disclaimer notice for TMDS implementation Updated Table 3 title to DVI-D/TMDS signals Included recommendation for display panel firmware detection for all TMDS based display interface type expected from the pluggable module Updated Table 3 and Table 4 HPD pins to be active high Included digital audio as the default audio if any of the digital display interface is being used	June 2012

Document Number	Revision Number	Description	Revision Date
		Updated Table 7 for COM1 as default UART port for the pluggable module Updated Table 8 PS_ON# for pulse width timing within 200ms	
324427	002	Updated Figure 1. Updated Table 1 pin assignment – removed HDMI term and replaced with DVI-D. Pin renamed to DVI_HPD, DVI_DDC_CLK, DVI_DDC_DATA, CEC. Updated Signal description for Table 3 DVI-D signals and Table 8 CEC signal. Updated airflow speed and ambient temperature requirements in the wind tunnel test. Updated the location of the imaginary plane for airflow speed measurement in the wind tunnel test.	April 2011
324427	001	Initial release.	October 2010

1 Introduction

1.1 Purpose and Scope

The purpose of this document is to describe the electrical, mechanical, and thermal specifications of the digital signage Open Pluggable Specification (OPS), which enables a standard and easier integration of a digital signage computing system or a pluggable module into the display panel. The scope covers the detailed electrical and connector specifications defined for the interoperability of the OPS, as well as the mechanical and thermal specifications that need to be adhered to when designing the physical system and its thermal solution.

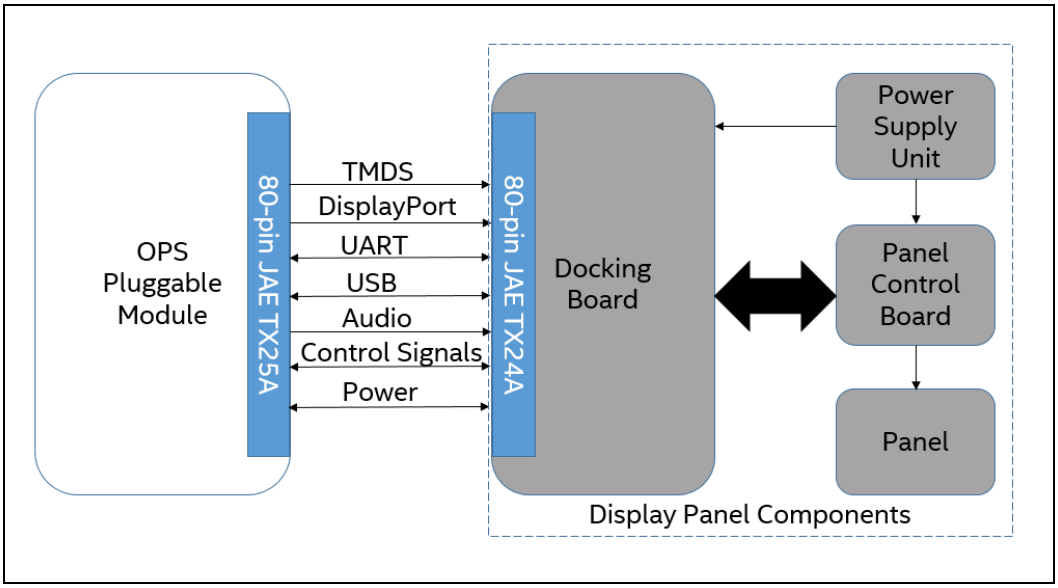
Note: *Throughout this document the digital signage computing system will be referred to as the "Pluggable Module".*

Throughout this document the 80pin JAE TX24A/TX25A series connector will be referred to as the "JAE connector".

Dimensions shown in all figures are in unit mm.

1.2 Overview

Figure 1. Functional Block Diagram



The OPS involves the integration concept of a Pluggable Module into the display panel thru a single and standard interfacing based on the 80 pin JAE plug and receptacle connectors. The power supply to the Pluggable Module together with the defined

feature interfaces are being routed through this set of connectors to provide a functional system level computing solution for digital signage.

The Pluggable Module consists of a computing board (for example, EPIC size board or smaller) in a wrapper chassis. The JAE connector enables plug and unplug mechanism between the Pluggable Module and the docking board inside the display panel.

Note: The connector does not support hot plug function. If such a requirement is needed, developers can choose to design the power-on self-start function and hot plug protection circuit to prevent any damage to the pluggable module and display panel docking board, which may be caused by the hot plug usage model.

1.3 Terminology

Table 1. Terminology

Term	Description
4K2K	4K2K resolution of display normally at 3840x2160 pixels
AC/DC	Alternating Current/Direct Current
AMT	Intel® Active Management Technology
CEC	Consumer Electronics Control, for Proof of Play/Display and panel detection
DDR	Double Data Rate – referring to random access memory (RAM)
DIMM	Dual In-line Memory Module
DP	DisplayPort
DVI-D	Digital Video Interface - Digital
EPIC	Embedded Platform for Industrial Computing (165mm x 115mm)
FAR	Free Area Ratio
GbE	Gigabit Ethernet
GPIO	General Purpose Input Output
LAN	Local Area Network
LV	Low Voltage
OPS	Open Pluggable Specification
PCIe*	PCI Express*
PoP	Proof of Play
RFID	Radio Frequency Identification technology
RJ45	Ethernet cable connector
SATA	Serial ATA
SSD	Solid State Drive
TMDS	Transition Minimized Differential Signaling

Term	Description
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
Wi-Fi*	Wireless IEEE 802.11 technology

1.4 Reference Documents

Table 2. Reference Documents

Document	Document No./Location
JAE TX24A/TX25A Connector Product Webpage	http://jae.com/jccom/en/connectors/detail/TX24A[s]TX25A/BoardToBoard
Whitepaper: Designing Intel® vPRO™ Technology Capable OPS Display Panels	http://download.intel.com/design/intarch/papers/327052.pdf?iid=6077
Thermal and Mechanical Design Guide: Digital Signage Open Pluggable Specification (OPS)	http://edc.intel.com/Link.aspx?id=3892
Design Guide: Pluggable Board and Docking Board Interconnect for Digital Signage Open Pluggable Specification (OPS)	http://edc.intel.com/Link.aspx?id=3974
Video: Introduction to the Intel® Open Pluggable Specification	http://www.intel.com/content/www/us/en/retail/retail-digital-signage-ops-animation.html

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2 Electrical and Connector Specification

2.1 Interface Connector Overview

The connector used for the Pluggable Module and the docking board interconnect is based on the JAE TX24A/TX25A family of plug and receptacle connectors. The JAE connector pins are capable of supporting up to a maximum current of 1A. For details, refer to the JAE connector datasheet or contact a JAE representative. The 80-pin right angle blind mate plug connector (p/n: TX25A-80P-LT-H1E) and its receptacle (p/n: TX24A-80R-LT-H1E) provide interfacing for the following features:

Power: DC IN +12V~+19V @ 8A max

Display Interface: DVI-D/TMDS† and DisplayPort

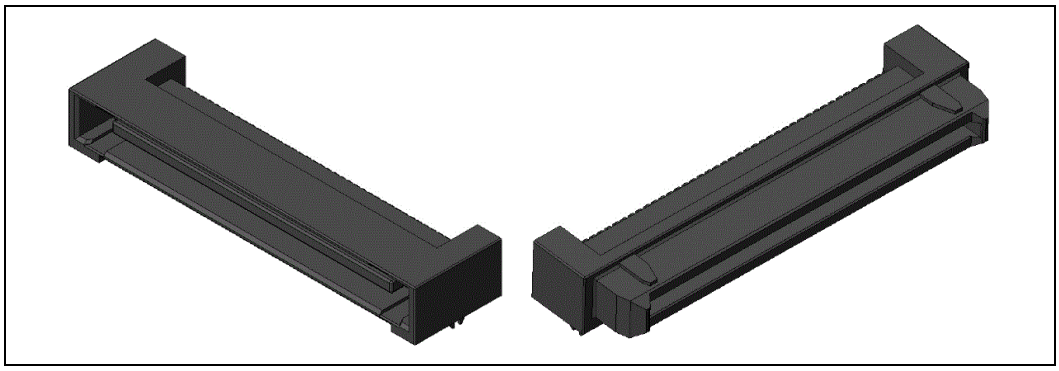
Audio: Left and Right Channel

USB: 3xUSB 2.0 (when USB3.0 is not used) or *2xUSB 2.0 and 1xUSB 3.0*

UART: Serial communication (Tx and Rx only)

Control Signals: Pluggable Module Power Status, Power ON via display panel, Pluggable Board Detect, Consumer Electronics Control (CEC), and System Fan Control.

Figure 2. JAE TX25A Plug and TX24A Receptacle Connectors



Note: Left: Plug connector (p/n: TX25A-80P-LT-H1E). Right: Receptacle connector (p/n: TX24A-80R-LT-H1E). Connector series image, reference only.

†User assumes full risk for using this specification, including use of any interface implementation other than the interface specified in this document. Refer also to the Notice section.

2.2 JAE Connector Compatibility

The 80-pin JAE TX24A and TX25A connector series are physically compatible with the existing 80-pin JAE TX24 and TX25 connector parts.

2.3 Pin Assignment

The JAE connector pin definition and assignment with regards to the features are listed in Table 3. The pin mapping indicated was based on the placement on the connector from top view as indicated in Figure 3.

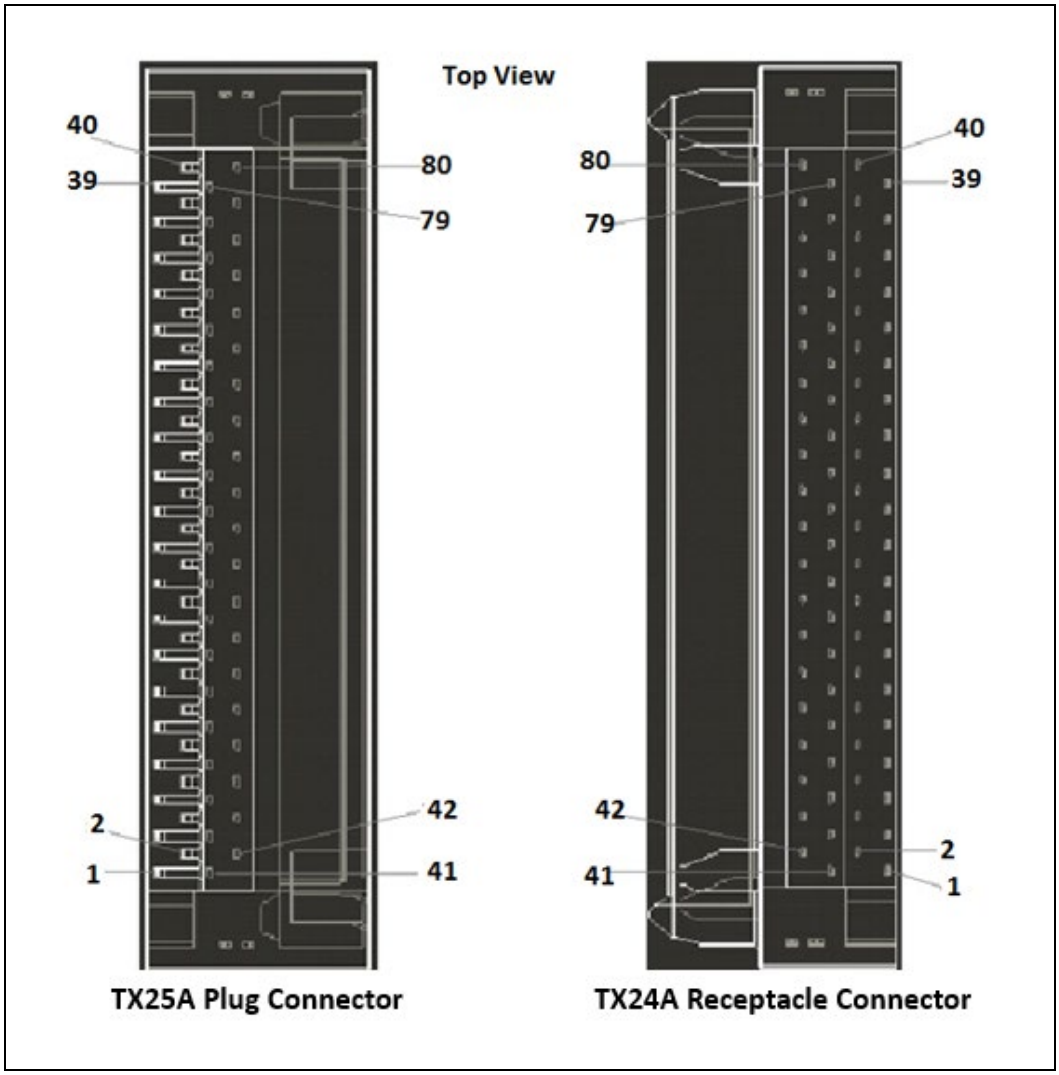
Table 3. Pin Assignment JAE TX24A/25A (80 Pins)

Pin No.	Signal	Description	I/O	Pin No.	Signal	Description	I/O
40	+12V~+19V	Power	-	80	GND	Ground	-
39	+12V~+19V	Power	-	79	GND	Ground	-
38	+12V~+19V	Power	-	78	GND	Ground	-
37	+12V~+19V	Power	-	77	GND	Ground	-
36	+12V~+19V	Power	-	76	GND	Ground	-
35	+12V~+19V	Power	-	75	GND	Ground	-
34	+12V~+19V	Power	-	74	PWR_STATUS	PowerGood	OUT (OC)
33	+12V~+19V	Power	-	73	PS_ON#	Pluggable Signal ON	IN
32	GND	Ground	-	72	PB_DET	Pluggable Board Detect	OUT
31	DVI_HPD	DVI-D	IN	71	CEC	Consumer Electronic Control	I/O
30	DVI_DDC_CLK	DVI-D	I/O	70	AZ_LINEOUT_R	Audio-Rch	OUT
29	DVI_DDC_DATA	DVI-D	I/O	69	AZ_LINEOUT_L	Audio-Lch	OUT
28	GND	Ground	-	68	GND	Ground	-
27	TMDS2+	DVI-D	OUT	67	USB_PP0	USB	I/O
26	TMDS2-	DVI-D	OUT	66	USB_PN0	USB	I/O
25	GND	Ground	-	65	GND	Ground	-
24	TMDS1+	DVI-D	OUT	64	USB_PP1	USB	I/O
23	TMDS1-	DVI-D	OUT	63	USB_PN1	USB	I/O
22	GND	Ground	-	62	GND	Ground	-
21	TMDS0+	DVI-D	OUT	61	USB_PP2	USB	I/O

Pin No.	Signal	Description	I/O	Pin No.	Signal	Description	I/O
20	TMDS0-	DVI-D	OUT	60	USB_PN2	USB	I/O
19	GND	Ground	-	59	GND	Ground	-
18	TMDS_CLK+	DVI-D	OUT	58	StdA_SSTX+	USB3.0	OUT
17	TMDS_CLK-	DVI-D	OUT	57	StdA_SSTX-	USB3.0	OUT
16	GND	Ground	-	56	GND	GND	-
15	DDP_HPD	DisplayPort	IN	55	StdA_SSRX+	USB3.0	IN
14	DDP_AUXP	DisplayPort	I/O	54	StdA_SSRX-	USB3.0	IN
13	DDP_AUXN	DisplayPort	I/O	53	GND	Ground	-
12	GND	Ground	-	52	UART_TXD	UART 3.3V	OUT
11	DDP_0P	DisplayPort	OUT	51	UART_RXD	UART 3.3V	IN
10	DDP_0N	DisplayPort	OUT	50	SYS_FAN	System Fan Control	OUT
9	GND	Ground	-	49	RSVD	Reserved pins	-
8	DDP_1P	DisplayPort	OUT	48	RSVD	Reserved pins	-
7	DDP_1N	DisplayPort	OUT	47	RSVD	Reserved pins	-
6	GND	Ground	-	46	RSVD	Reserved pins	-
5	DDP_2P	DisplayPort	OUT	45	RSVD	Reserved pins	-
4	DDP_2N	DisplayPort	OUT	44	RSVD	Reserved pins	-
3	GND	Ground	-	43	RSVD	Reserved pins	-
2	DDP_3P	DisplayPort	OUT	42	RSVD	Reserved pins	-
1	DDP_3N	DisplayPort	OUT	41	RSVD	Reserved pins	-

1. The I/O column definition is in reference to the pluggable board.
2. OC = Open Collector.
3. For USB3.0 implementation, pins #60 and #61 shall be used to complement the Super Speed USB signals.

Figure 3. JAE TX24A/25A Connector Pin Layout



2.4 Signal Description

This section provides a detailed description of each signal passing through the JAE connector. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type with regards to the pluggable board:

I Input Pin

O Output Pin

OC Open Collector Output Pin.

The "Type" for each signal is indicative of the functional operating mode of the signal.

2.4.1 Power and Ground

Table 4. Power and Ground Signals

Pin No.	Name	Type	Description
33, 34, 35, 36, 37, 38, 39, 40	+12V~+19V	-	The Pluggable Module supports a voltage range of +12V~+19V DC IN (mandatory). The maximum total current rating shall not exceed 8A (1A per pin). **The in-rush current of the pluggable module shall not exceed 10A to ensure successful power up operation.** *It is mandatory for the Pluggable Module (OPS) manufacturers to provide a Power Rating label on the Pluggable Module and/or product brief/catalog which indicates the power consumption of the module (e.g., 40W). Display manufacturers must indicate the power supply spec for OPS on the product brief/catalogue (e.g., 16V/4A).*
3, 6, 9, 12, 16, 19, 22, 25, 28, 32, 53, 56, 59, 62, 65, 68, 75, 76, 77, 78, 79, 80	GND	-	Ground

2.4.2 Display Interface

Table 5. DVI-D/TMDS† signals

Pin No.	Name	Type	Description
31	DVI_HPD	I	DVI Hot Plug Detect. Active High
30	DVI_DDC_CLK	I/O	Display Data Channel Signals DVI Control Data and Clock. These are single ended control signals used for communications between the chipset DVI display port and a panel device (Sink).
29	DVI_DDC_DATA		
27	TMDS2+	O	TMDS Data Channel
26	TMDS2-		
24	TMDS1+		
23	TMDS1-		
21	TMDS0+		
20	TMDS0-		
18	TMDS_CLK+	O	TMDS Clock Channel
17	TMDS_CLK-		

Note: Recommended for display panel firmware to include detection of all TMDS based type of display interfaces to avoid interoperability-related issues.

Table 6. Display Port Signals

Pin No.	Name	Type	Description
15	DDP_HPD	I	Display Port Hot Plug Detect. Active High
14	DDP_AUXP	I/O	Display Port Auxiliary Channel
13	DDP_AUXN		
11	DDP_0P	O	Display Port Data Channel
10	DDP_0N		
8	DDP_1P		
7	DDP_1N		
5	DDP_2P		
4	DDP_2N		
2	DDP_3P		
1	DDP_3N		

†User assumes full risk for using this specification, including use of any interface implementation other than the interface specified in this document. Refer also to the Notice section.

2.4.3 Audio

Table 7. Audio Signals

Pin No.	Name	Type	Description
70	AZ_LINEOUT_R	O	Audio Right Channel
69	AZ_LINEOUT_L	O	Audio Left Channel

Note: These audio signals will be used when DVI-D is implemented/used. By default, if any of the digital display interface type is being used (for example, DisplayPort), then the audio source shall be from the digital audio within the DP channel.

2.4.4 USB Interface

Table 8. USB Signals

Pin No.	Name	Type	Description
67	USB_PP0	I/O	USB2.0 Differential Pair
66	USB_PN0		
64	USB_PP1		
63	USB_PN1		
61	USB_PP2		
60	USB_PN2		
58	StdA_SSTX+	O	USB3.0 SuperSpeed Transmitter Differential Pair
57	StdA_SSTX-		
55	StdA_SSRX+	I	USB3.0 SuperSpeed Receiver Differential Pair
54	StdA_SSRX-		

2.4.5 UART Interface

Table 9. UART signals

Pin No.	Name	Type	Description
52	UART_TXD	O	Transmitted UART data from pluggable board, UART 3.3V LVTTL signal. Assign as COM 1 for the UART Port in the pluggable module
51	UART_RXD	I	Received UART data for pluggable board, UART 3.3V LVTTL signal. Assign as COM 1 for the UART Port in the pluggable module

2.4.6 OPS Control Interface

Table 10. Control signals

Pin No.	Name	Type	Description
74	PWR_STATUS	OC	Power status indication signal or Power Good status of the pluggable board. This pin shall be Open Collector and pull up to +3.3V on the docking/control board side. High: Pluggable board power off state Low: Pluggable board power on state See Figure 4 for illustration example.
73	PS_ON#	I	Pluggable Signal ON: This is meant for signal initiation to power ON or boot up the Pluggable Module. PS_ON# shall be asserted at least 500 ms after power is delivered from PSU to the board via the JAE connector (G3 to S5 state). Pull up to +3.3V on the pluggable board. **A pulse width present on the PS_ON# shall be detected and responded within 200 ms to ensure successful operation.** Use case: Power Button initiation from the panel control board to the Pluggable board via, for example, IR remote control ON. The PWRBTN# pin on the Intel ICH/PCH can be utilized for this purpose. PWRBTN# has a 16 ms of internal debounce logic. External debouncing circuit is not required. Refer to the respective platform design guide and chipset datasheet.

Pin No.	Name	Type	Description
			+If the pluggable board present state is S5, the transitions start as soon as the PWRBTN# is pressed (but after the debounce logic), and does not depend on when the Power Button is released. +If pluggable board present state is S0-S4 and if PWRBTN# is held low for at least four consecutive seconds, this will initiate unconditional transition to S5 state. **This timing spec applies only for Intel ICHx series and 5 series chipset. For other platforms, refer to the respective component Power Button spec. Refer to Figure 5 for illustration example.
72	PB_DET	O	Pluggable board detection. Output signal, recommend grounded on the pluggable board side with pull up to +3.3V on the docking/control board side High: No Pluggable Low: Pluggable board Present Refer to Figure 6 for illustration example.
71	CEC	I/O	Consumer Electronics Control for Proof of Play/Display initiative. Can also be used for display panel status detection and other control functions. The display panel control CPU shall support this functionality.
50	SYS_FAN	O	System Fan: This signal shall be used to control the display panel system fan. Recommended pull up +3.3V on docking board side and routed to the system fan control. High: System Fan OFF Low: System Fan ON *1 Note *1: This signal shall be triggered ON by the thermal management system (EC) in the pluggable module only when needed. Use case: In situation where display panel is in standby mode and the Pluggable Module is still operating (e.g., remote maintenance, etc.), system fan solution may still be needed and since display panel is in standby mode there is no way to control the system fan. This pin therefore serves as an option to trigger the system fan to operate when necessary.

2.4.7 Reserved

Table 11. Reserved Pins

Pin No.	Name	Type	Description
41, 42, 43, 44, 45, 46, 47, 48, 49	RSVD	-	These pins are RESERVED for future expansion and shall be left as No Connect (NC).

Figure 4. Illustration of PWR_STATUS Implementation Example

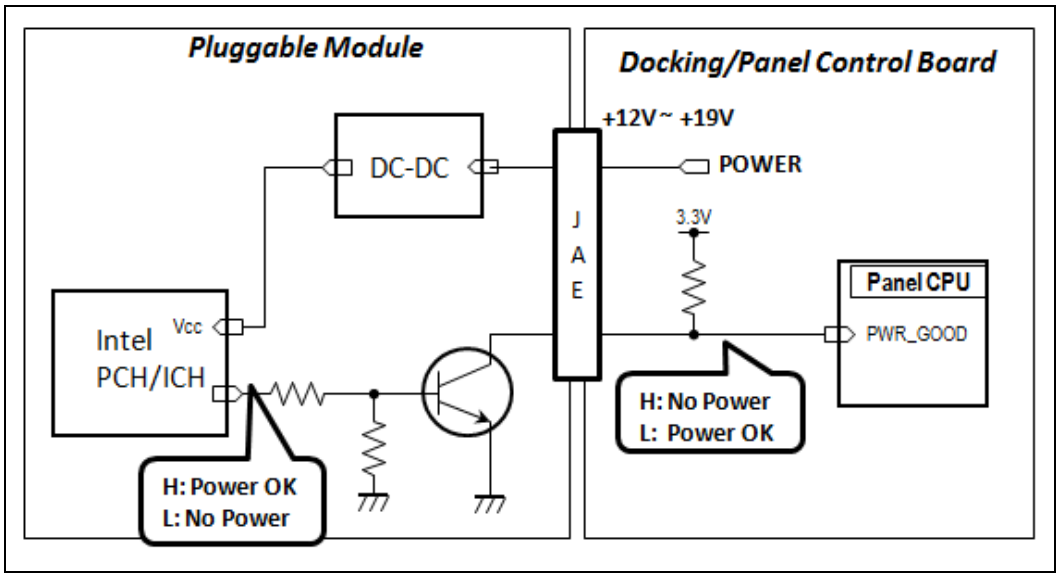


Figure 5. Illustration of PS_ON# Implementation Example

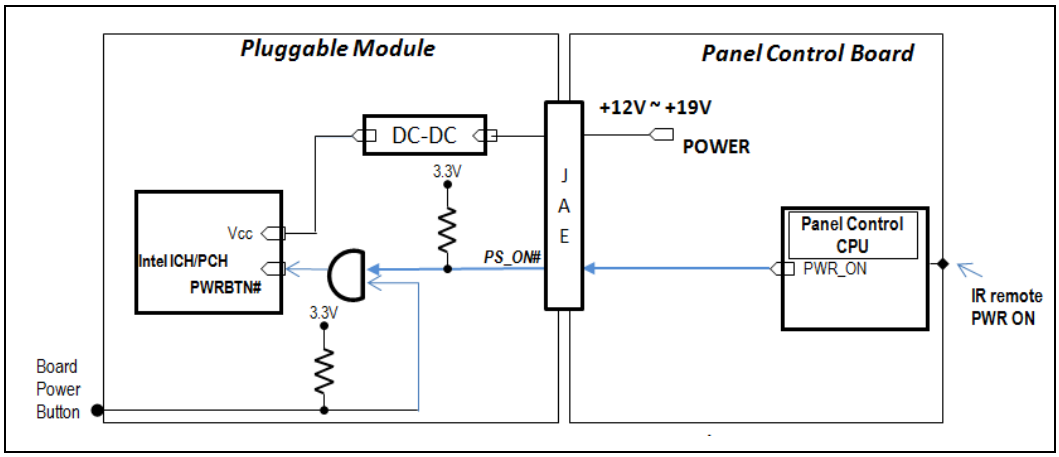
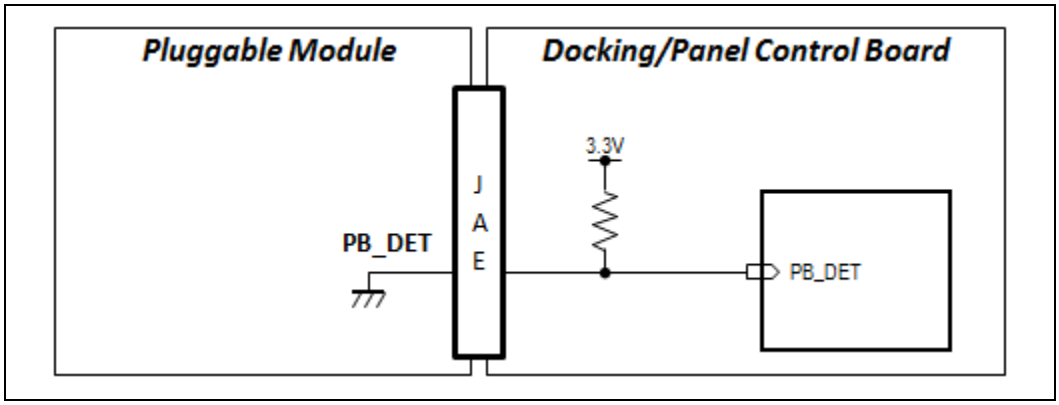


Figure 6. Illustration of PB_DET Implementation Example



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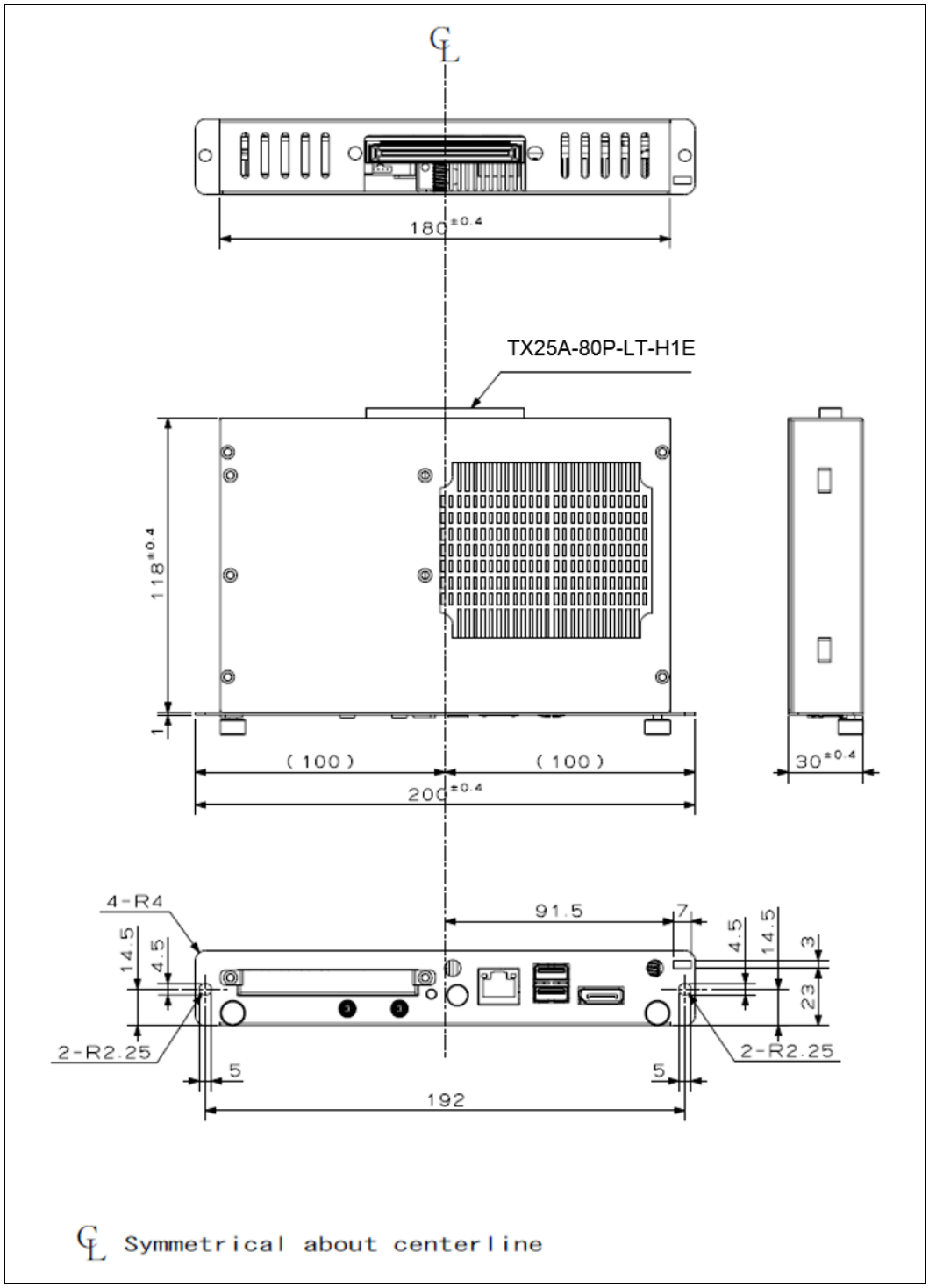
3 Mechanical Specification

3.1 Physical Dimension of the Pluggable Module

Figure 7 shows the dimensions of the Pluggable Module. The overall dimension of the module including the mounting frame is 200 mm x 119 mm x 30 mm. Figure 7 also shows the dimension and location of the front panel screw holes as well as the security lock. For the precise location of the JAE plug connector (TX25A) refer to Figure 8.

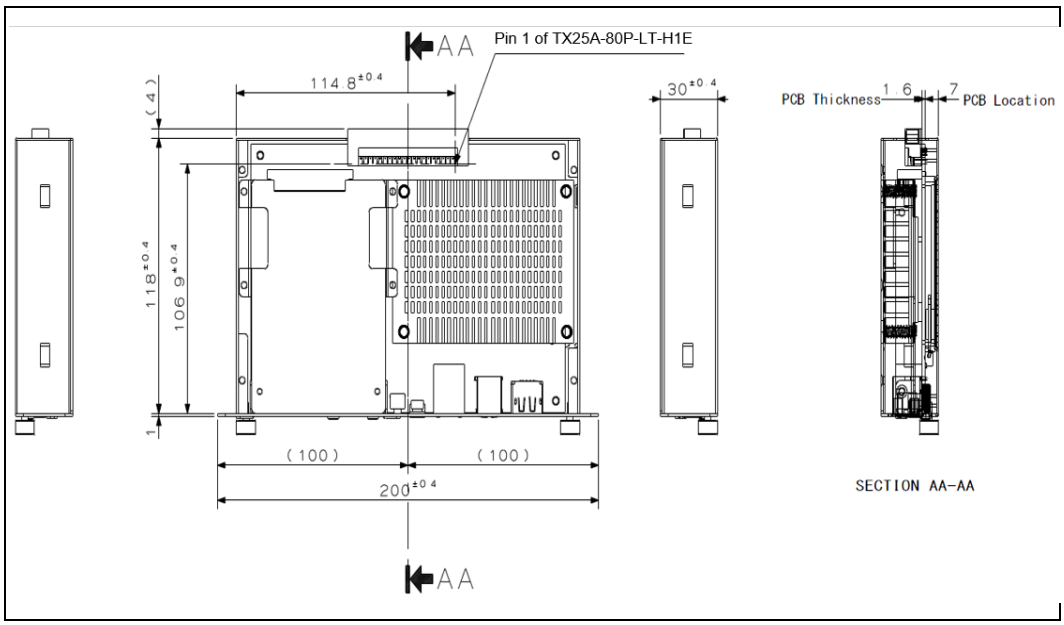
Figure 7. Dimensions of the Pluggable Module



3.2 Location of the JAE Plug Connector

Figure 8 shows the detailed location of the JAE TX25A plug connector. Pin 1 of the connector is located at 114.8 mm from the edge of the module, and 106.9 mm from the inner side of the front panel. For mating tolerance of TX25A plug connector and TX24A receptacle connector, refer to the JAE specification.

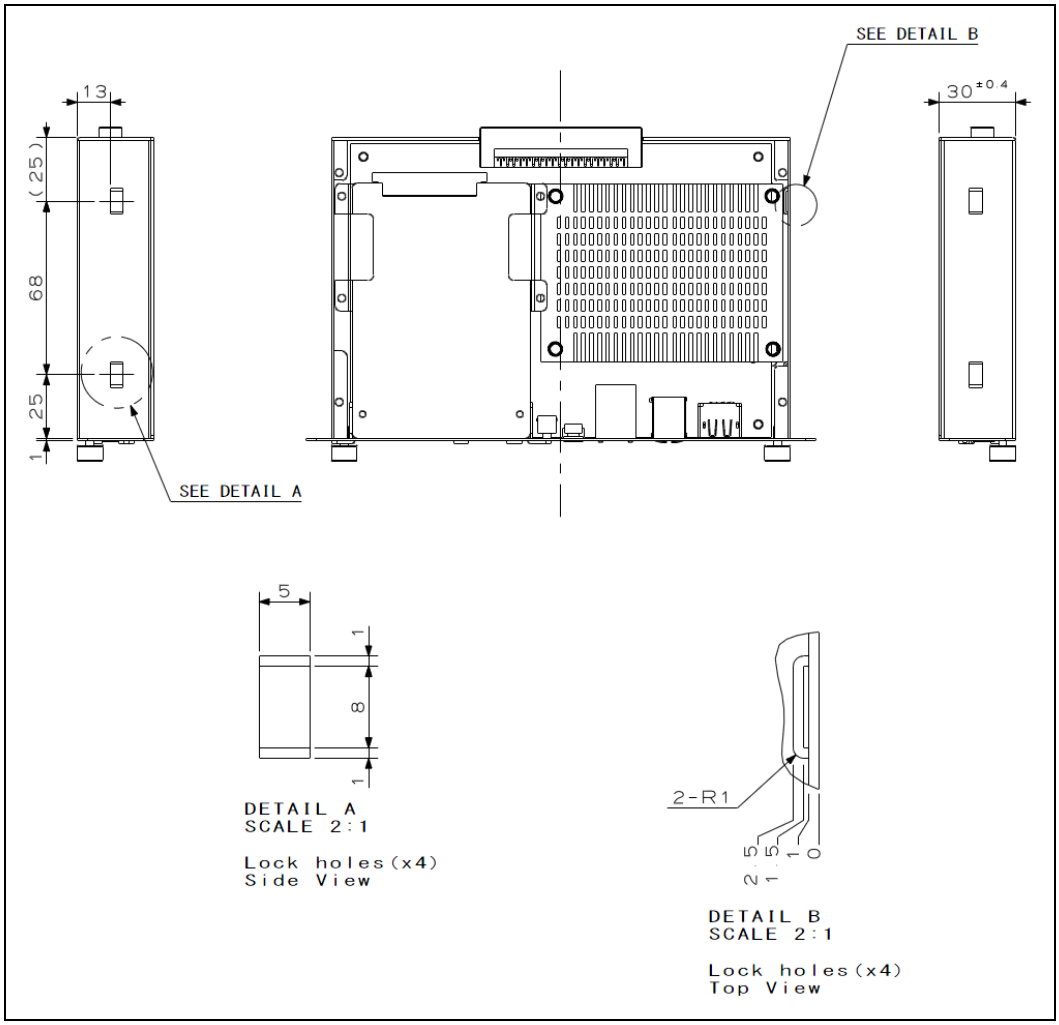
Figure 8. Location of JAE TX25A Plug Connector



3.3 The Lock Holes on the Pluggable Module

There are two lock holes on each side of the Pluggable Module. These holes, mated with the matching lock pins from the guiding rail on the display system, provide locking effect to the module during docking/undocking process. Figure 9 shows the dimension and the location of these locks holes on the Pluggable Module. Guiding rail implementation has to adhere to the location of the lock holes, as well as the thickness and depth of the Pluggable Module.

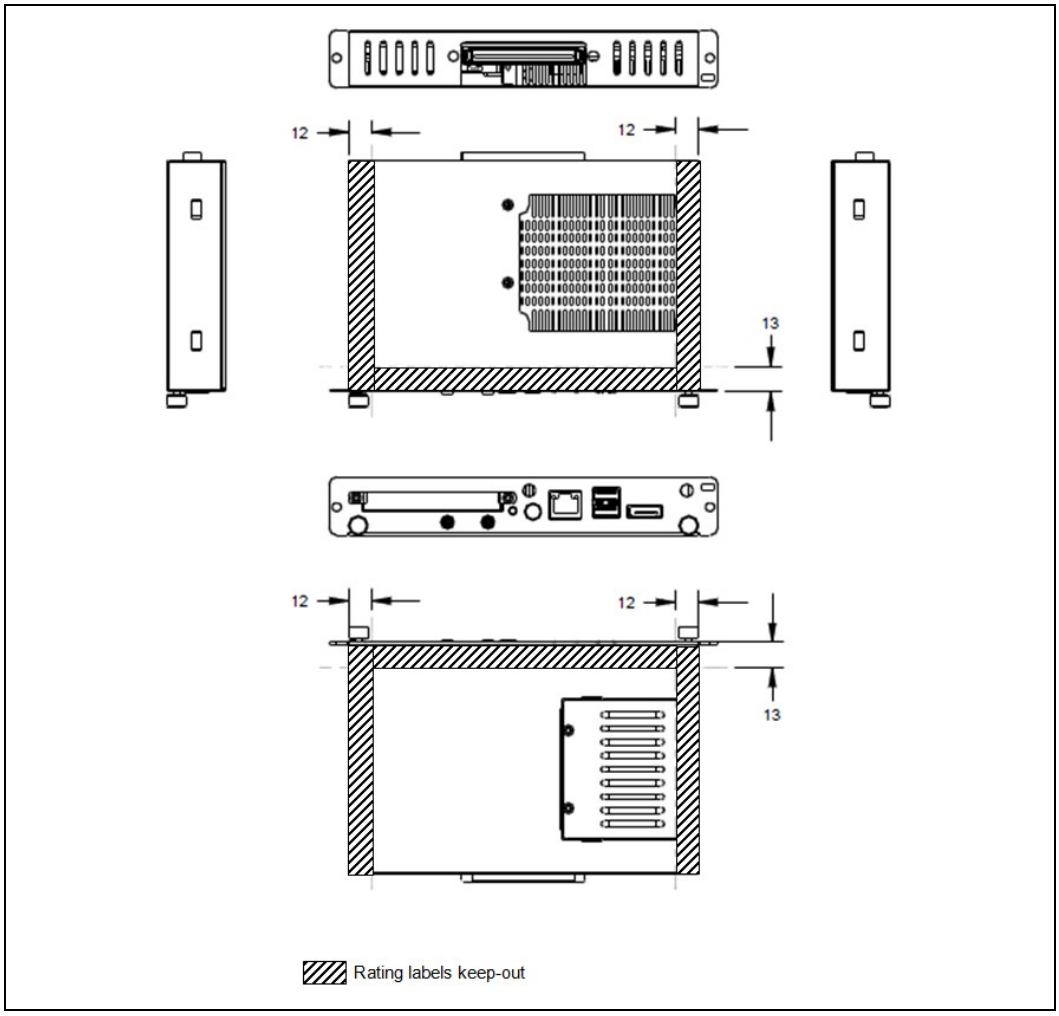
Figure 9. Location of Lock Hole on the Pluggable Module



3.4 Rating Labels

Rating labels ***should not*** be placed on keep-out-zones on the Pluggable Module due to potential interference with the guiding mechanism that guides the module box during the mating/un-mating process. The dimensions of these keep-out-zones are shown in Figure 10. Also, the rating labels ***should not*** be placed on the ventilation holes on the heat sink and the DIMM service windows, as that would prevent air intake to the components.

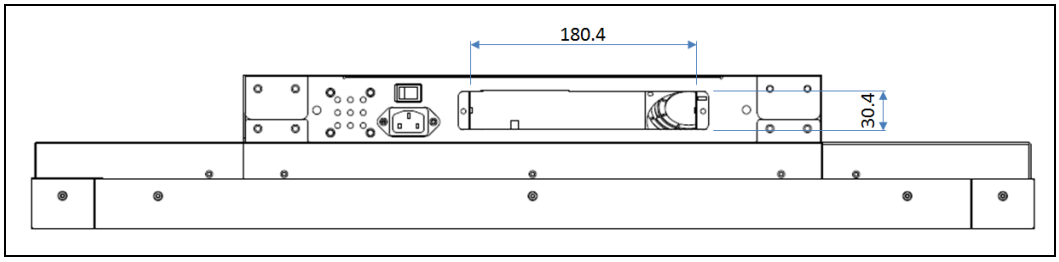
Figure 10. Keep-out-zones for the Rating Labels



3.5 Dimensions of the Pluggable Module Slot on the Display Panel

Figure 11 shows the location of the module slot on a reference display panel. Here, the module plugs in from the bottom of the display panel. However, it can either be plugged in from the bottom, or from the side of the display panel. It is imperative that the module slot be big enough to accommodate the Pluggable Module so that it plugs in smoothly. Therefore, the slot should be at the maximum manufacturing tolerance of the module as indicated in Figure 7.

Figure 11. Minimum Dimension of the Module Slot on a Reference Display Panel



3.6 Venting Area on the Display Panel for the Pluggable Module

Vent holes must be opened at the location of the Pluggable Module so that air can enter the heat sink on top of the module. It is required that the venting area should at least cover the Pluggable Module so that the entire top surface is exposed to ambient air. Figure 12 shows the minimum venting area for the Pluggable Module in a reference display panel. Note that Figure 12 is only an illustration for the venting area for modules that plug in from the bottom the display panel. For modules that plug in from the side, the orientation of the venting area should follow accordingly as shown in Figure 13.

Figure 12. Minimum Dimension of the Venting Area on a Reference Display Panel (module plugs in from bottom of the display panel)

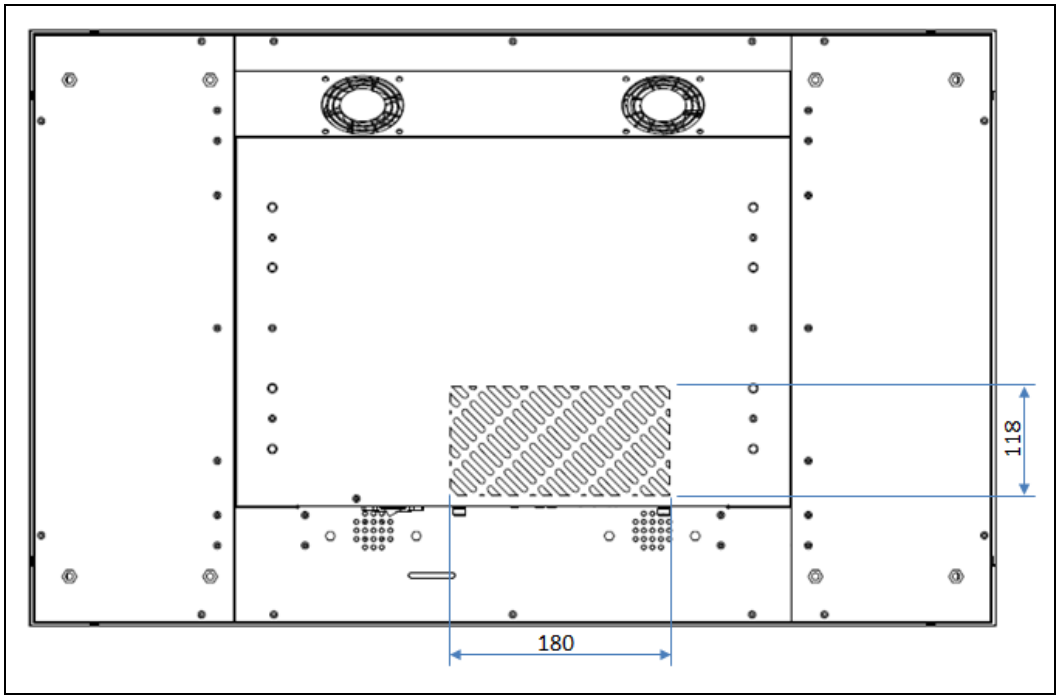
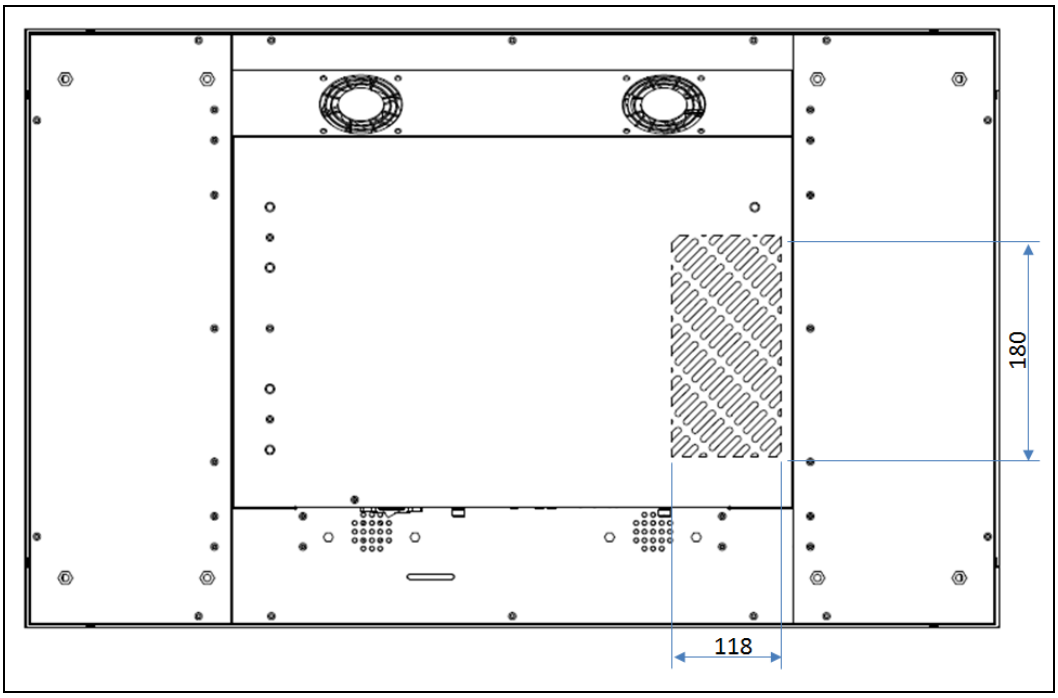


Figure 13. Minimum Dimension of the Venting Area on a Reference Display Panel (module plugs in from right side of the display panel)



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4 Thermal Specifications

4.1 Thermal Management for the Pluggable System

The thermal management of the Pluggable Module must be handled carefully to ensure all components comply with the thermal specifications. This section illustrates a simple wind tunnel test to quantify the airflow needed for module cooling. Figure 14 shows the top view of an empty wind tunnel. (The module should not be present in this test.) There is an opening at the top where air from the surrounding enters the wind tunnel. The Free Area Ratio (FAR) for the opening is set to 0.6 for reference. It is imperative that all other surfaces be sealed off so that air enters the wind tunnel only from the top opening. Figure 14 also shows an imaginary plane located approximately at the mid-section of the wind tunnel. It is required that the average airflow speed through this plane is ***1.2m/s*** to ensure sufficient airflow is provided to the module for forced convection cooling.

Figure 15 shows the wind tunnel dimension and the location of the module. The module can be tested in an environment temperature ***not higher than 45°C*** to ensure all components pass the thermal requirement. It is the responsibility of module designer to ensure all components comply with the thermal specification.

Figure 14. Wind Tunnel Test (No Pluggable Module Present in This Setup)

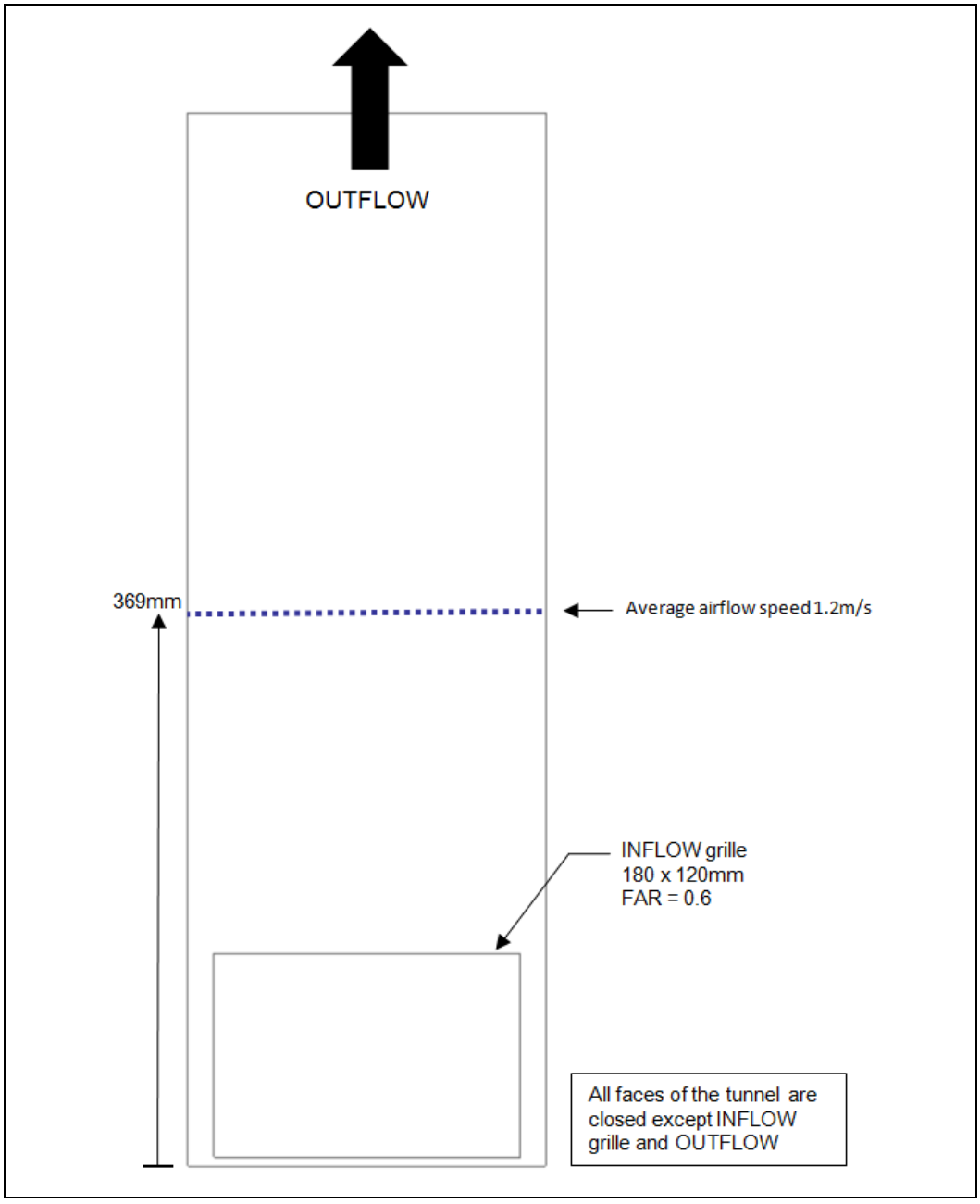
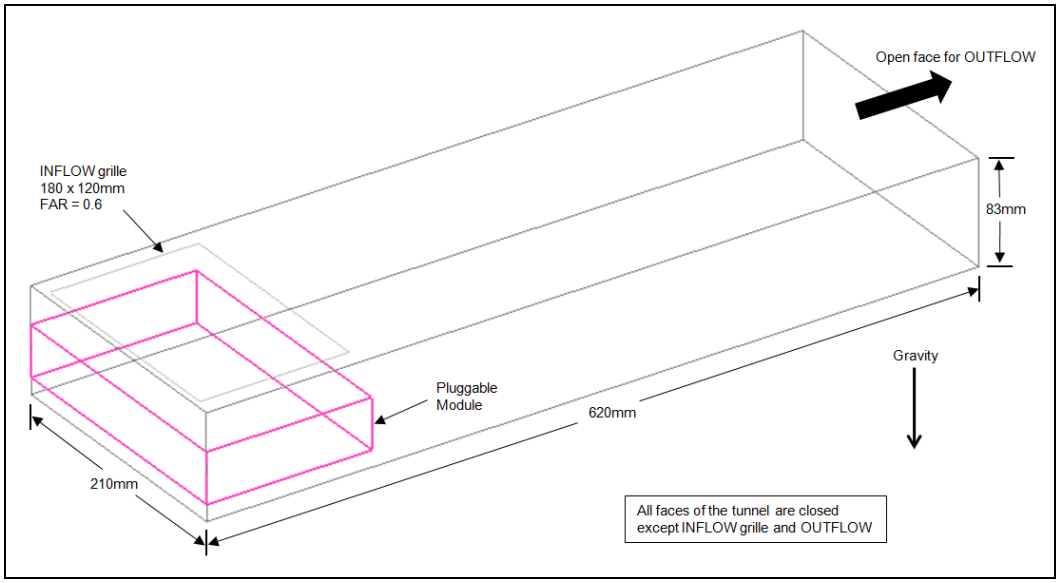


Figure 15. Wind Tunnel Dimension and Location of the Pluggable Module



4.2 Thermal Consideration for Display Panel

The display panel should be designed in such a way that there is sufficient airflow provided to the Pluggable Module within the panel in the desired operating environment. The operating temperature and airflow being provided to the Pluggable Module are keys to good thermal design. While there are vast varieties of possible display panel design, it is hard to achieve a point solution that satisfies the Pluggable Module and display panel thermal requirements. However, the display panel design must ensure the thermally critical components in the Pluggable Module are meeting their thermal requirements.

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